**A Novel Approach for Parallel CRC generation for high speed application**

**ABSTRACT**

High speed data transmission is the current scenario in networking environment. Cyclic redundancy check (CRC) is essential method for detecting error when the data is transmitted. With challenging the speed of transmitting data, to synchronize with speed, it’s necessary to increase speed of CRC generation. Starting from the serial architecture identified a recursive formula from which parallel design is derived. This paper presents 64 bits parallel CRC architecture based on F matrix with order of generator polynomial is 32. Proposed design is hardware efficient and required 50% less cycles to generate CRC with same order of generator

polynomial. The whole design is functionally verified using Xilinx ISE Simulator.

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis